Novel nanotube multi-quantum dot devices (Supporting Information)

R. Tormo-Queralt,^{†,¶} C. B. Møller,^{†,¶} D. A. Czaplewski,[‡] G. Gruber,[†] M. Cagetti,[†]

S. Forstner,[†] N. Urgell-Ollé,[†] J. A. Sanchez-Naranjo,[†] C. Samanta,[†] C. S. Miller,[‡] and A. Bachtold^{*,†}

†ICFO - Institut De Ciencies Fotoniques, The Barcelona Institute of Science and Technology, 08860 Castelldefels (Barcelona), Spain

‡Center for Nanoscale Materials, Argonne National Laboratory, Argonne, IL, 60439, USA ¶These authors contributed equally to the work

E-mail: adrian.bachtold@icfo.eu

1. Detailed fabrication process

The process starts with a high resistivity [100] silicon wafer (> $10k\Omega cm$) with 315 nm of thermal grown SiO₂. We use a bilayer PMMA process for lift-off of metal to use as alignment marks for the patterning of the device. On the wafer, poly methyl methacrylate (PMMA) with a molecular weight of 495 kDa at a concentration of A3 (as purchased from Kayaku Advanced Materials) is spun at 2 krpm for 60 s at 500 rpm/s acceleration and baked at 180 °C for 5 min. After cooling, a second layer is spun of PMMA 950k A6 at 4 krpm for 60 s at 500 rpm/s acceleration and baked at 180 °C for 5 min. The wafer is exposed in a JEOL 8100FS using 2 nA of current and a dose of $1000 \mu C/cm^2$. After exposure, the resist is developed in MIBK 1:3 isopropyl alcohol (IPA) at ~ 20 °C for 2 min with sonication, rinsed in IPA for 30 s and then blown dry with N₂. The wafer is exposed to an O₂ plasma using 50 W of power at a pressure of 175 mTorr for 30 s to

improve adhesion to the substrate. Metal (5 nm Ti / 60 nm Pt) is electron beam evaporated on the wafer using a Temescal 2000 evaporator. For resist lift-off, the wafer is soaked in 1165 at 75 °C overnight. Then the wafer is spray rinsed with deionized (DI) water, rinse in running DI water, sonicated in DI water for 2 min, spray rinsed in DI water, rinsed in running DI water and blown dry with N2. It is then sonicated in acetone for 2 min, rinsed with IPA and blown dry with N₂. The same bilayer PMMA spincast and baking process is used to pattern the next two sets of electrodes. The first set of electrodes is patterned using the Jeol 8100 using 2 nA of current at a dose of $1550 \,\mu\text{C/cm}^2$. After exposure, the resist is developed in MIBK 1:3 IPA at 3.7 °C for 2 min with sonication, rinsed in IPA at 3.7 °C for 30 s and then blown dry with N₂. The wafer is exposed to an O₂ plasma using 50 W of power at a pressure of 175 mTorr for 30 s. Metal (5 nm Ti / 60 nm Pt) is electron beam evaporated on the wafer. The same lift-off process is used. The second set of electrodes is patterned using the same resist, exposure, metal deposition, and lift-off processes. To pattern the bond pads and larger features, optical lithography is used. Shipley S1813 is spun at 4 krpm for c at 500 rpm/s acceleration and baked on a hotplate at 115 °C for 90 s. The wafer is exposed in a Heidelberg MLA 150 with 450 nm light at a dose of 120 mJ/cm^2 . The wafer is developed in MIF 351 mixed 1:4 with DI water with agitation, rinsed in DI and blown dry with N₂. The wafer is exposed to an O₂ plasma using 50 W of power at a pressure of 175 mTorr for 30 s. Metal (5 nm Ti / 100 nm Pt) is electron beam evaporated on the wafer. The same lift-off process is used. To pattern the taller source and drain electrodes that suspend the nanotube over the other gates, the same PMMA resist, exposure, development and cleaning steps are used. A thicker metal is evaporated (5 nm Ti / 100 nm Pt) and then the wafer is allowed to cool for 30 min followed by another evaporation of 70 nm of Pt. The same PMMA lift-off procedure is followed. In order to create the ridge structures, the wafer is etched in an Oxford Plasmalab 100 system flowing 50 sccm of CHF3 and 2 sccm of O_2 while maintaining a pressure of 10 mTorr at 20 °C with 100 W of RF power for 15 min to remove \sim 160 nm of SiO₂. To ensure no polymer accumulation on the Pt electrodes, the wafer is cleaned for 5 min in an O₂ plasma at 100 W of power, similar to the descum step after resist development. To isolate the electrodes to prevent shorting of spurious

nanotubes to other gates, we deposit SiO_2 as a protective layer. ZEP 520A (Zeon corporation) is spun on the wafer at 1 krpm for 60 s using 500 rpm/s acceleration and then baked at 150 °C for 3 min. The wafer is exposed in the Jeol 8100 using 2 nA and a dose of $350 \,\mu\text{C/cm}^2$. The wafer is developed in n-amyl acetate for 60 s while sonicating, rinsed in IPA and blown dry with N₂. 50 nm of SiO₂ is deposited in an Oxford HDCVD plasmalab 200 system using 20 sccm of N₂O, 8.5 sccm of SiH₄ at 2.5 mTorr and 100 °C for 150 s. The same lift-off process is used to remove the resist. The pattern to create the catalyst islands uses the PMMA spin cast process. The wafer is exposed in the Jeol 8100 using 2 nA of current and a dose of $1000 \,\mu C/\mu m^2$. The resist is developed in MIBK 1:3 IPA at $\sim 20\,^{\circ}\text{C}$ for 2 min with sonication, rinsed in IPA for 30 s and then N_2 dried. Subsequently, 50 nm of SiO₂ are deposited using a Lesker LAB18 e-beam evaporator. This layer later serves as sacrificial layer to lift off catalyst particles and dicing debris. The wafer is then diced into 7.5 mm by 7.5 mm chips which each contain 49 multigate devices. The chips are cleaned in O₂ plasma and the catalyst for nanotube growth is drop casted on the chip. The catalyst is synthesised by mixing 80 mg of Fe(NO₃)₃ · 9H₂O, 4 mg of MoO₂(C₅H₇O₂)₂ and 60 mg Al₂O₃ in a solution of 60 mL of methanol. The chip with catalyst is soaked in acetone overnight to dissolve the PMMA and the sacrificial SiO₂ is lifted off. The chip is rinsed in IPA and blown dry in N₂, leaving the catalyst solution only in the pre-patterned rectangles near the gates (see main text, Figs. 1c,d). After a short O_2 plasma cleaning step, the chip is ready for the CVD.

We grow carbon nanotubes using a standard fast-heating CVD technique at 900 °C.¹ For the growth step, we place the chip in a quartz spoon inside a standard 1 inch diameter quartz tube. We insert the tube together with the chip in a Lindeberg Blue Mini-Mite tube furnace and start heating up to the growth temperature (900 °C) under a constant flow of 100 sccm of H₂ and 500 sccm of Ar. H₂ gas creates a reducing atmosphere optimal for the nanotube growth. When heating up the furnace we keep the chip outside the heating area. Once we reach the growth temperature, we set the CH₄ flow to 550 sccm, insert the section of the tube with the chip in the heating area and leave it for 6 minutes. During this step, nanotubes grow from the catalyst islands in random directions under the influence of the gas flow dynamics, some of them bridging the gate electrodes. After

the growth step, we switch off the furnace heater and turn off the CH_4 flow but keep the other gases until the temperature reaches 180 °C. Devices are then selected using a probe station at room temperature in air and then in vacuum to find suspended nanotubes with a small band gap and a two-terminal a resistance < $150 k\Omega$ at negative gate voltage.

2. Charge noise finite element model simulations

The impact of potential charge fluctuators is assessed by finite element simulation. We model the nominal geometries of a selection of devices using COMSOL and simulate their electrostatic landscape. The model of the device shown in Fig. 1a can be seen in Fig. 1b of the main text. The model contains a 4 nm diameter metallic rod that describes the nanotube and that is suspended from source and drain electrodes 140 nm above gate electrodes. The electrodes sit upon a 300 nm thick SiO_2 layer on a high resistivity Si wafer. All electrodes are grounded. In this particular layout, gates are separated by 90 nm and all electrode edges are rounded with a 25 nm radius of curvature. A single electron point charge, indicated as a red dot in Fig. 1b, is placed on the surface of the SiO_2 layer directly below the nanotube and in between the gates. Charge noise affecting quantum dots in the nanotube would result from spatial fluctuations of this point charge.

The metal electrodes screen the electric field emanating from the charge. This results in a position dependent electric potential felt by the nanotube. This can be see in Fig. 3a of the main text, which is a simulation of the electrostatic potential of a nanotube suspended over the nominal geometry of the device shown in Fig. 2a. This field is largest immediately above the charge and smallest closest to the source and drain electrodes. As the etch depth in between the gates is increased, the potential charge fluctuator is moved further away which increases the screening caused by the gate electrodes. At large etch depths a slight modulation of the electrostatic potential becomes apparent reflecting the gate electrode pitch.

The impact of a fluctuating charge is not distributed equally along the nanotube. This is assessed by computing the change in the electrostatic potential along the nanotube per unit of charge displacement in a particular direction. The effect of moving the charge 10 nm directly into the SiO_2 layer can be seen by comparing the solid and dashed lines in Fig. 3a. By taking the difference of two such curves, calculated with a 2 nm displacement, and normalizing by the displacement, we calculate the potential gradient along the nanotube. In general it is not straightforward to relate the fluctuations of the electrostatic potential along the nanotube with its impact on an embedded quantum dot system. Nonetheless the qualitative impact may be estimated by evaluating the maximum value of the potential gradient along the nanotube.

Device geometry can significantly reduce the impact of a fluctuating charge. This is clear from Fig. 3b where the maximum potential gradient at the nanotube is exponentially suppressed as the etch depth in between the gates is increased. We compare the results from the two devices shown in Fig. 2. The characteristic length scale of the exponential suppression is 29.0 nm for the larger device geometry and 17.6 nm for the smaller device. The more compact geometry of Fig. 2b features a reduced potential gradient seen by the nanotube even at zero etch depth. Both the shorter characteristic length scale and the reduced potential gradient at zero etch depth are due to increased screening of the closer gate electrodes. We fit an exponential decay plus a constant background since we observe a noisy background in the calculated electrostatic potential gradient when the potential is small. We attribute this constant background to meshing variations. The increased suppression with larger etch depth displayed by the simple case illustrated in Fig. 3b is also seen for charges moving in other directions, such as the parallel or perpendicular directions with respect to the gates.

An increased suppression is also observed for a charge located elsewhere. In Fig. S1 we consider a charge located below the central gate electrode on the sidewall of the trench. Despite being in close proximity to the gate electrode, the electrostatic potential induced along the nanotube is on the same order of magnitude as a charge fixed in between the gates. This may be seen from the solid lines in Fig. S1a. Even at significant trench depth d the size of the electrostatic potential remains comparable. Moving the charge down by 2 nm gives rise to the dashed lines of Fig. S1a. Just as in the main text, we calculate the electrostatic potential gradient by comparing these two curves and normalizing by the displacement.

The magnitude of electrostatic potential gradient decreases with increasing trench depth. Fig-



Figure S1: (a) The simulated electrostatic potential along the nanotube created by one electron in the oxide. Solid lines are with the charge (red dot) on the SiO_2 sidewall below the central gate for various etching depths. Dashed lines show the potential when the charge is moved 2 nm down. The schematic of the device cross-section includes the nanotube in yellow, the electron as a coloured dot, the metal electrodes in dark grey, the SiO_2 in grey, and the SiO_2 etching depth *d*. (b) The largest value of the electrostatic potential gradient (absolute value) along the nanotube as a function of the etching depth *d*. The red curve corresponds to a charge situated on the sidewall and at the bottom of the trench (red dot in schematic). The blue curve corresponds to a charge on the sidewall fixed in place at 2 nm below the gate electrode (blue dot in schematic).

ure S1b shows two curves corresponding to two situations. For the red curve the charge is on the sidewall at the bottom of the trench (red dot in Fig. S1b), while for the blue curve the charge remains 2 nm below the electrodes (blue dot in Fig. S1b). For the charge fixed 2 nm below the gate the gradient drops modestly and eventually saturates at large trench depths. For the charge at the bottom of the trench the gradient decreases substantially as the trench depth is increased. The overall behaviour is similar to that of a charge placed in between the gates as considered in the main text. However, there is a dip in the potential gradient caused by a change in the sign of the gradient. This may be understood in the following way. For a charge located on the trench sidewall, there are two competing effects in the potential gradient variation. The first is the decreased screening experienced by the charge when moving further away from the gate electrode. This effect is dominant for charges in close proximity to the gate electrode. The second effect is the increased screening of the gate array at greater distance from the nanotube. This effect on the potential gradient is dominant at large trench depths. Both effects result in potential gradient variations with opposite sign. When the trench depth becomes comparable to the gate separation, both effects tend to cancel each other. At greater trench depths the gradient continues to decrease just as for a charge in between two gates discussed in the main text.

3. Scanning electron microscopy characterization of Device 1

The layout of Device 1 and the position of the nanotube are determined by scanning electron microscopy. One of the many images taken with a 30 kV acceleration voltage is shown in Fig. S2. From these images the orientation, placement and slack of the nanotube is determined. Additionally, the precise dimensions of all trenches and electrodes, including their rounded edges, are quantified. Our simulations show that the nanotube has different capacitive couplings to gates G2 and G4 due to the asymmetric electric field between the nanotube and the two wide electrodes (shown in the image) that connect the gates and the contact pads.



Figure S2: Scanning electron micrograph of *Device 1* (main text). The slack and the angle of the nanotube with respect to the electrodes are taken into account in our electrostatic potential simulations.

4. Details on devices shown in main text

Device summary												
Figure	NT-gate	Gate widths (nm)					Electrode separation (nm)					
	(nm)	G1	G2	G3	G4	G5	S-G1	G1-G2	G2-G3	G3-G4	G4-G5	G5-D
Fig1a	140	80	100	80	100	80	100	90	90	90	90	100
Fig1c	100	80	100	80	100	80	100	90	90	90	90	100
Fig1d	100	50	80	50	80	50	60	85	100	100	85	60
Fig2a	100	80	100	80	100	80	100	90	90	90	90	100
Fig2b	100	40	40	40	40	40	60	60	60	60	60	60
Fig4a	140	80	100	80	100	80	100	90	90	90	90	100
Fig4b	140	80	150	80	150	80	120	115	120	120	115	120

Table S1: Summary of the relevant dimensions of the devices discussed in the main text.

References

 Huang, S.; Cai, X.; Liu, J. Growth of millimeter-long and horizontally aligned single-walled carbon nanotubes on flat substrates. *Journal of the American Chemical Society* 2003, *125*, 5636–5637.